ABSTRACT OF THE DISCLOSURE

In the control section, an operation instruction not prescribing a functional specification, and a unit for processing the specific application-purpose operation instruction is provided within the processor core. The structure of this unit can be changed based on a flexible pipeline structure, and is separately designed for each application field. A register that prescribes a latency from when an instruction of the above unit is issued till when a result can be utilized is also provided in the processor core so as to prevent contention of an output port. Another register that prescribes a latency relating to a constraint of an interval of issuing an instruction of the above unit is also provided in the processor core so as to prevent contention of a resource with the preceding instructions.